MMBT4403L, SMMBT4403L

Switching Transistor

PNP Silicon

Features

- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

ON Semiconductor®

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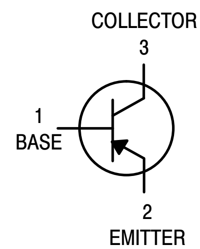
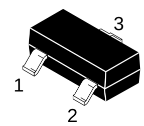
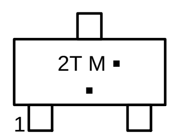




SOT−23 (TO−236)
CASE 318
STYLE 6

MARKING DIAGRAM



2T = Specific Device Code*
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Specific Device Code, Date Code or overbar orientation and/or location may vary depending upon manufacturing location. This is a representation only and actual devices may not match this drawing exactly.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	−40	Vdc
Collector−Base Voltage	V_{CBO}	−40	Vdc
Emitter−Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Continuous	I_C	−600	mAdc
Collector Current − Peak	I_{CM}	−900	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board (Note 1) @T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) @T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Transient pulses must not cause the junction temperature to be exceeded.
1. FR−5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

ORDERING INFORMATION

Device	Package	Shipping†
MMBT4403LT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel
SMMBT4403LT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel
MMBT4403LT3G	SOT−23 (Pb−Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

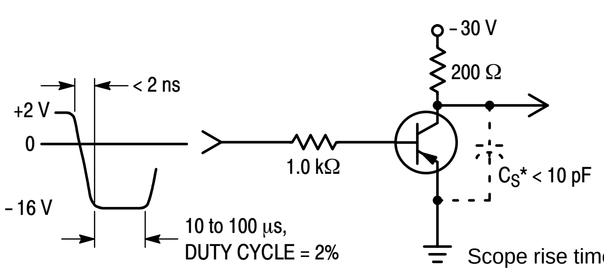
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

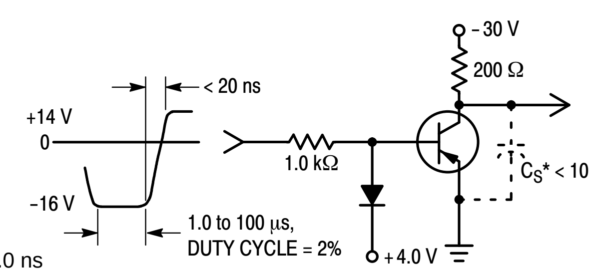
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (Note 3)	(I_C = −1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−40	−	Vdc
Collector−Base Breakdown Voltage	(I_C = −0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	−40	−	Vdc
Emitter−Base Breakdown Voltage	(I_E = −0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	−	Vdc
Base Cutoff Current	(V_{CE} = −35 Vdc, V_{EB} = −0.4 Vdc)	I_{BEV}	−	−0.1	μAdc
Collector Cutoff Current	(V_{CE} = −35 Vdc, V_{EB} = −0.4 Vdc)	I_{CEX}	−	−0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			−
	(I_C = −0.1 mAdc, V_{CE} = −1.0 Vdc)		30	−	
	(I_C = −1.0 mAdc, V_{CE} = −1.0 Vdc)		60	−	
	(I_C = −10 mAdc, V_{CE} = −1.0 Vdc)		100	−	
(Note 3)	(I_C = −150 mAdc, V_{CE} = −2.0 Vdc)		100	300	
(Note 3)	(I_C = −500 mAdc, V_{CE} = −2.0 Vdc)		20	−	
Collector−Emitter Saturation Voltage (Note 3)		$V_{CE(sat)}$			Vdc
	(I_C = −150 mAdc, I_B = −15 mAdc)		−	−0.4	
	(I_C = −500 mAdc, I_B = −50 mAdc)		−	−0.75	
Base−Emitter Saturation Voltage (Note 3)		$V_{BE(sat)}$			Vdc
	(I_C = −150 mAdc, I_B = −15 mAdc)		−0.75	−0.95	
	(I_C = −500 mAdc, I_B = −50 mAdc)		−	−1.3	
SMALL−SIGNAL CHARACTERISTICS					
Current−Gain − Bandwidth Product	(I_C = −20 mAdc, V_{CE} = −10 Vdc, f = 100 MHz)	f_T	200	−	MHz
Collector−Base Capacitance	(V_{CB} = −10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	−	8.5	pF
Emitter−Base Capacitance	(V_{BE} = −0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{eb}	−	30	pF
Input Impedance	(I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{ie}	1.5	15	kΩ
Voltage Feedback Ratio	(I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{re}	0.1	8.0	X 10^{-4}
Small−Signal Current Gain	(I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{fe}	60	500	−
Output Admittance	(I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{oe}	1.0	100	μMhos
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = −30 Vdc, V_{EB} = −2.0 Vdc, I_C = −150 mAdc, I_{B1} = −15 mAdc)	t_d	−	15	ns
Rise Time		t_r	−	20	
Storage Time	(V_{CC} = −30 Vdc, I_C = −150 mAdc, I_{B1} = I_{B2} = −15 mAdc)	t_s	−	225	ns
Fall Time		t_f	−	30	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

SWITCHING TIME EQUIVALENT TEST CIRCUIT





Scope rise time < 4.0 ns
*Total shunt capacitance of test jig connectors, and oscilloscope

Figure 1. Turn−On Time

Figure 2. Turn−Off Time

TRANSIENT CHARACTERISTICS

—— 25°C – – – 100°C

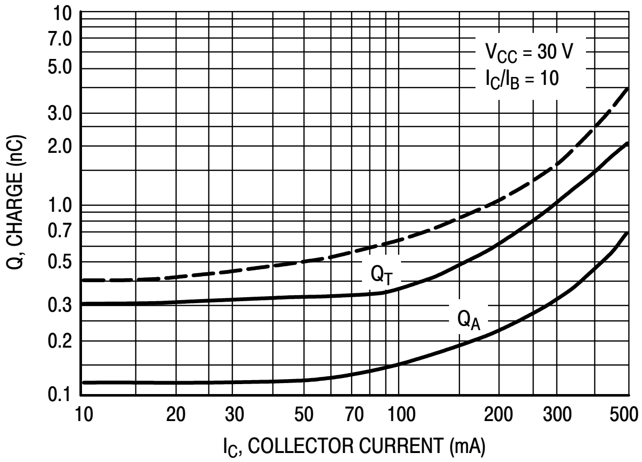


Figure 3. Charge Data

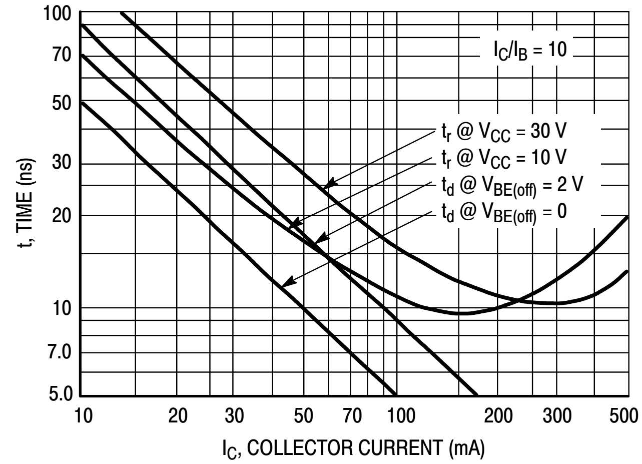


Figure 4. Turn−On Time

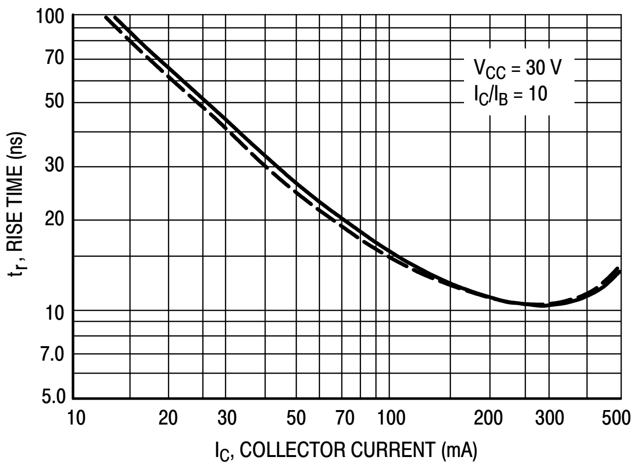


Figure 5. Rise Time

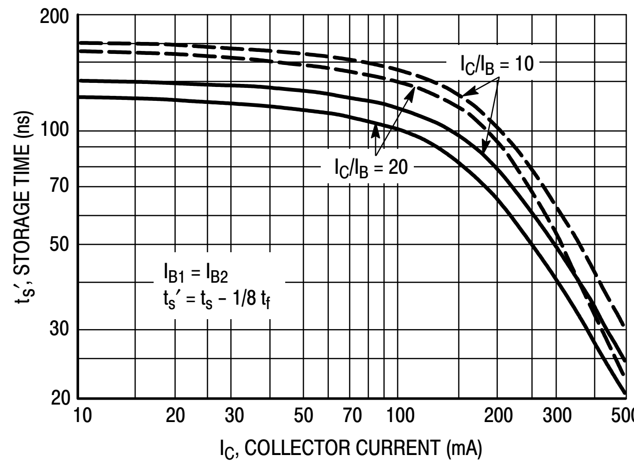


Figure 6. Storage Time

SMALL−SIGNAL CHARACTERISTICS NOISE FIGURE

V_{CE} = −10 Vdc, T_A = 25°C; Bandwidth = 1.0 Hz

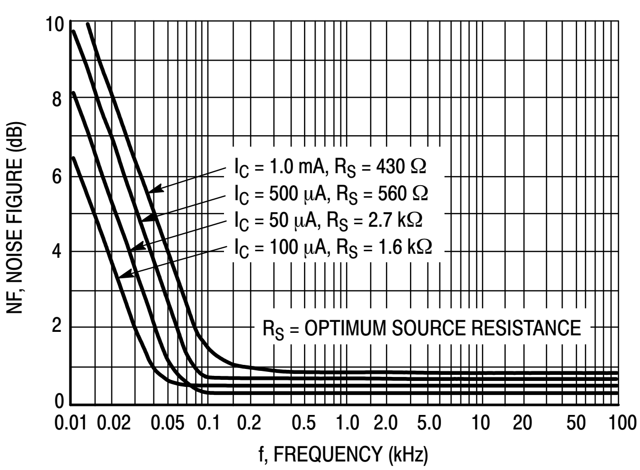


Figure 7. Frequency Effects

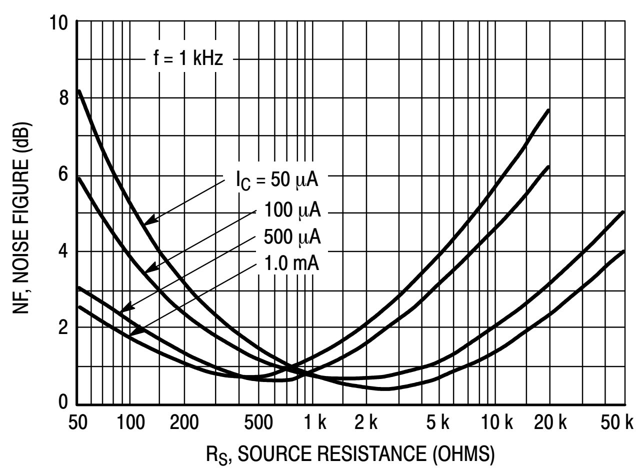


Figure 8. Source Resistance Effects

h PARAMETERS

V_{CE} = 10 Vdc, f = 1.0 kHz, T_A = 25°C

This group of graphs illustrates the relationship between h_{fe} and other "h" parameters for this series of transistors. To obtain these curves, a high−gain and a low−gain unit were selected from the MMBT4403LT1 lines, and the same units were used to develop the correspondingly numbered curves on each graph.

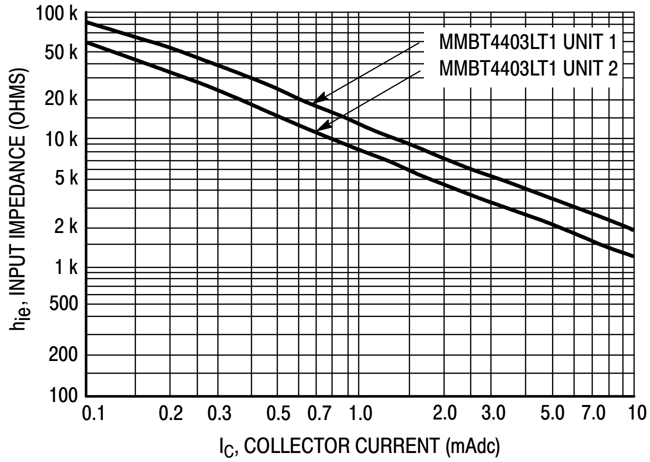


Figure 9. Input Impedance

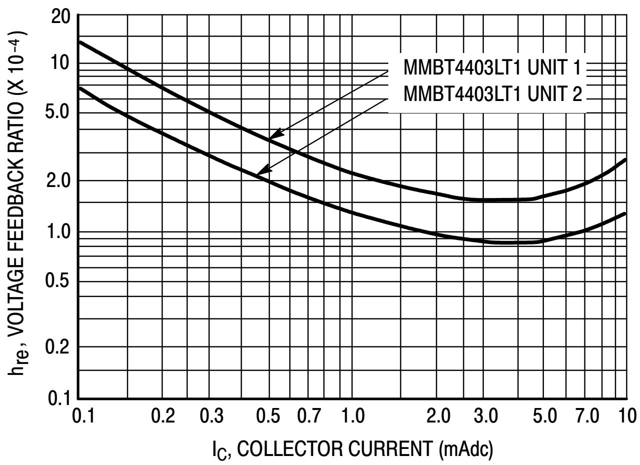


Figure 10. Voltage Feedback Ratio

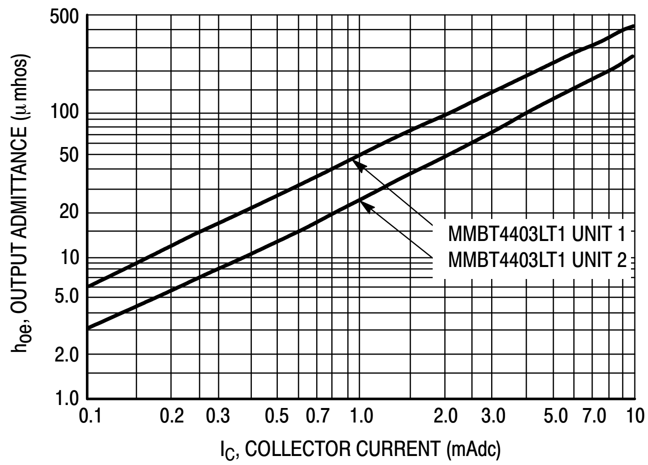


Figure 11. Output Admittance

STATIC CHARACTERISTICS

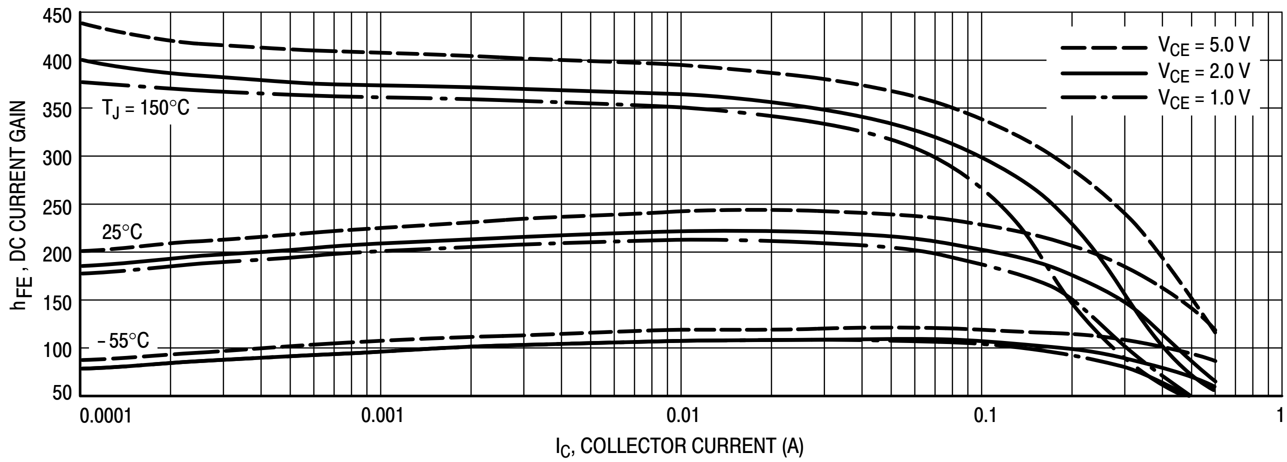


Figure 12. DC Current Gain

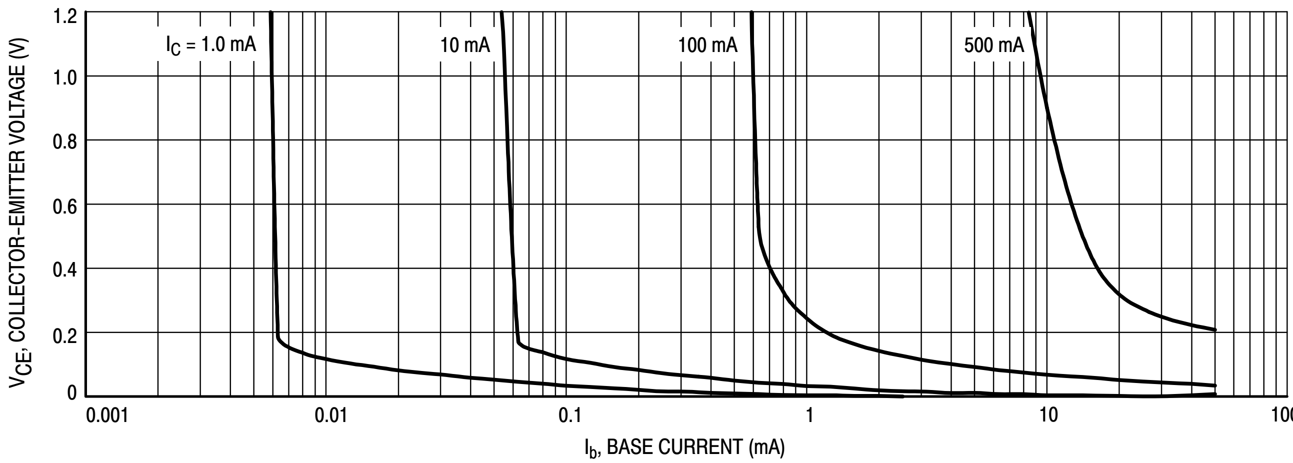


Figure 13. Collector Saturation Region

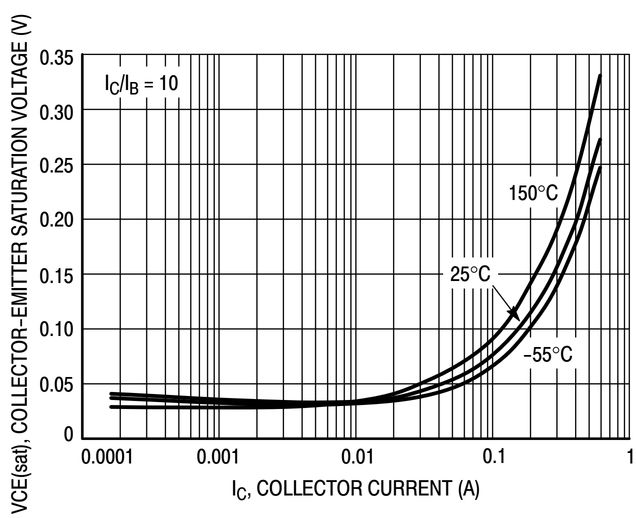


Figure 14. Collector−Emitter Saturation Voltage vs. Collector Current

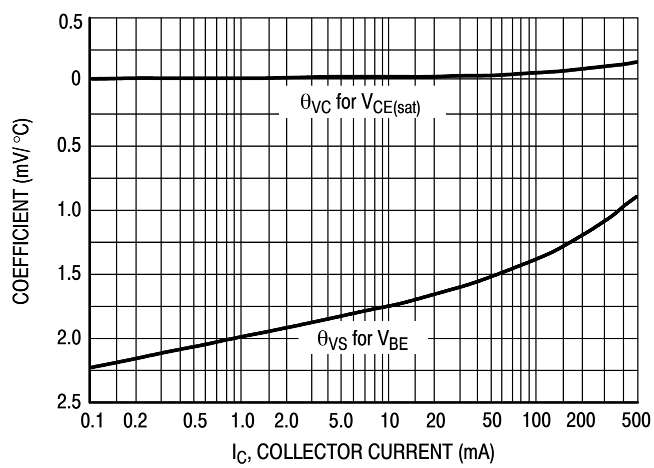


Figure 15. Temperature Coefficients

STATIC CHARACTERISTICS

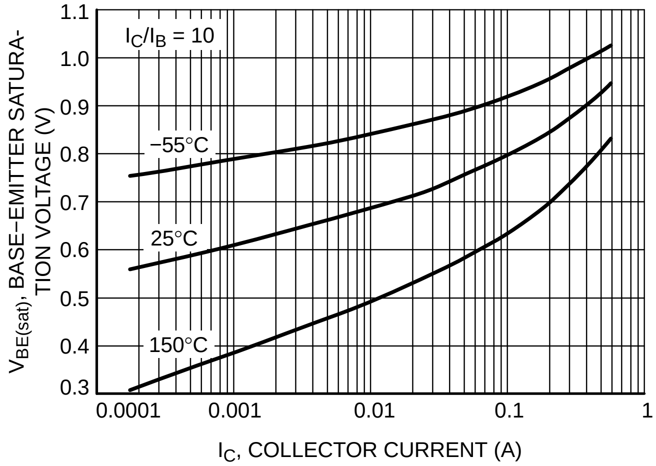


Figure 16. Base−Emitter Saturation Voltage vs. Collector Current

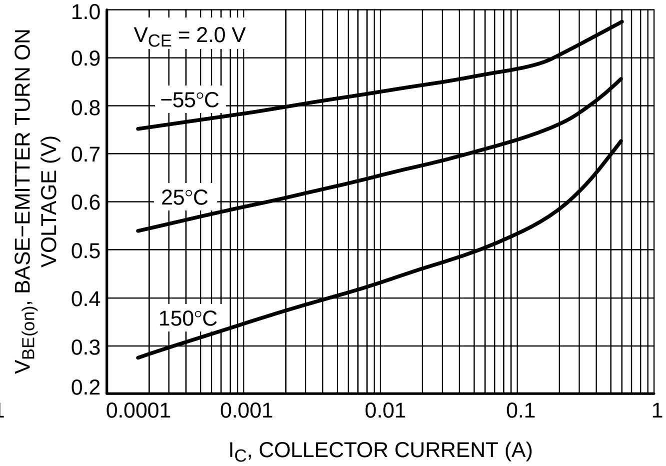


Figure 17. Base−Emitter Turn On Voltage vs. Collector Current

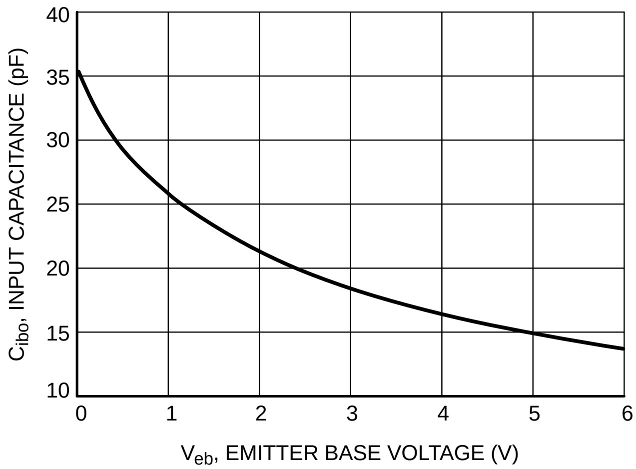


Figure 18. Input Capacitance vs. Emitter Base Voltage

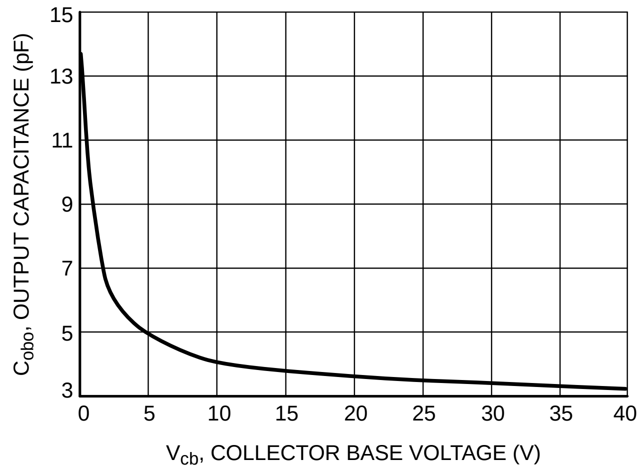


Figure 19. Output Capacitance vs. Collector Base Voltage

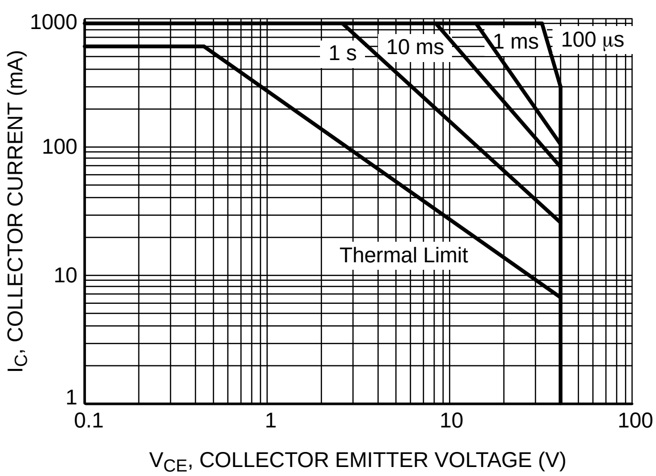


Figure 20. Safe Operating Area

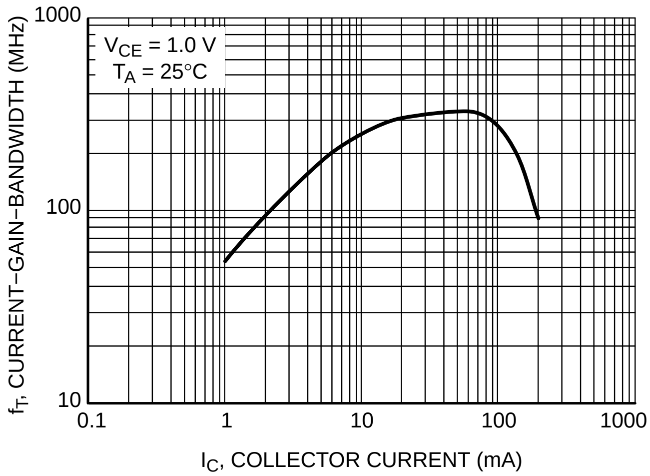
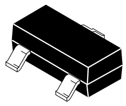


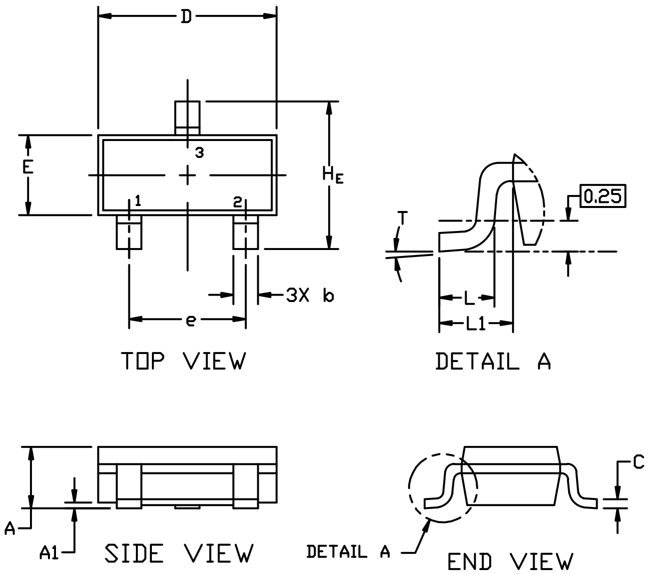
Figure 21. Current−Gain−Bandwidth Product



SCALE 4:1

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

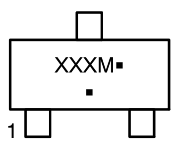


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

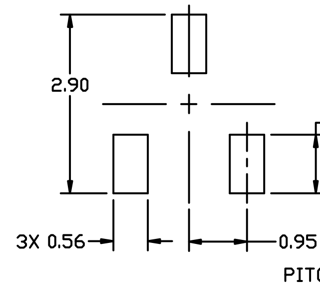
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−23 (TO−236)**	**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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